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Mihai Telescu, Noël Tanguy, Pascale Bréhonnet, Pierre Vilbé, Léon-Claude Calvez. Low Complexity Equivalent Circuit Models for VLSI Interconnects. 10th IEEE Workshop on Signal Propagation on Interconnects, May 2006, Berlin-Mitte, Germany. pp.271-274. hal-00468947

HAL Id: hal-00468947

<https://hal.univ-brest.fr/hal-00468947>

Submitted on 1 Apr 2010

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Low Complexity Equivalent Circuit Models for VLSI Interconnects

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Abstract

In this paper we present a technique for generating low complexity equivalent circuit models for VLSI circuit interconnects via the Laguerre-Gram model order reduction (MOR) method developed by our team. We discuss model passivity and equivalent circuit implementation and then show the advantages of our method in preserving important signal parameters such as rise time, delay and overshoot.

Introduction

In 1965, Gordon Moore, one of the founding fathers of Intel made a prediction on the integration density of future circuits estimating that the number of transistors per circuit would double every eighteen months. This estimation, which we have come to know as Moore's law, has proven quite accurate. Moreover, circuits become ever smaller and ever faster while reducing their energy consumption. It is under these circumstances that interconnect effects such as delay, distortion, noise, reflections need to be taken into consideration by circuit designers. But simulation time is also an important issue and generating both precise and time efficient models has become a research topic of major interest for both the industrials and academia. Our team has explained the details of the Laguerre-Gram MOR method [1] as well as certain improvements we may bring when it is specifically used for interconnect lines. A frequency approach on the method and a pre-processing technique is presented in [6] while [2] and [5] describe a heuristic iterative algorithm which may be used to improve reduced model accuracy. Therefore we do not insist on the method itself in this paper and content our selves to a general presentation in paragraph II. We discuss two key issues: model passivity and equivalent circuit synthesis (paragraphs III and IV) and give an example comparing the accuracy of a Laguerre-Gram reduced model with a classical PEEC (Partial Element Equivalent Circuit) model in paragraph V.

Model order reduction method

Laguerre-Gram MOR is essentially a rational approximation technique. Its main steps when dealing with a single-dimensional system are: 1) decomposition of the original transfer function $\hat{f}(s)$ in a Laguerre series; 2) construction of an approximation basis $\Omega_r = \{\hat{f}_0, \hat{f}_1, \dots, \hat{f}_r\}$ by repeated applications of the Λ operator; 3) construction of a rational model $\tilde{\hat{f}}(s)$. The robustness and speed of the algorithm is mainly due to the Λ operator defined by:

$$\begin{aligned}\hat{f}_0(s) &= \hat{f}(s), \\ \hat{f}_{i+1}(s) &\triangleq \Lambda \hat{f}_i(s) \\ &= \left[\hat{f}_i(s) - (2\alpha)/(s+\alpha) \hat{f}_i(\alpha) \right] (s+\alpha)/(s-\alpha)\end{aligned}$$

It should also be noted that system stability is preserved.

In practice we usually model multidimensional systems described by matrices of transfer functions such as the one given below

$$Y(s) = \begin{bmatrix} \hat{y}^{(11)}(s) & \hat{y}^{(12)}(s) & \dots & \hat{y}^{(1m)}(s) \\ \hat{y}^{(21)}(s) & \hat{y}^{(22)}(s) & \dots & \hat{y}^{(2m)}(s) \\ \dots & \dots & \dots & \dots \\ \hat{y}^{(p1)}(s) & \hat{y}^{(p2)}(s) & \dots & \hat{y}^{(pm)}(s) \end{bmatrix}$$

The reduction procedure for each element in this case is basically the same, but we need to impose a common denominator on elements if we want to find an equivalent RLCG circuit.

$$\tilde{\hat{y}}^{(\lambda, \mu)}(s) = \frac{n^{(\lambda, \mu)}(s)}{D(s)} \text{ avec } 1 \leq \lambda \leq p \quad 1 \leq \mu \leq m$$

For reasons of simplicity in the case of VLSI interconnects we use admittance matrices [2],[5].

Passivity enforcement

Interconnect lines are passive systems and therefore their reduced order rational models must be passive in order to insure the stability of the systems they are part of. If the model is not passive we need to impose this constraint a posteriori, in other words to "correct" the model. One solution was proposed by Gustavsen and Semlyen [4]. It relies upon the correction of the negative eigenvalues of the $G(\omega)$ matrix where $G = \text{Re}\{Y\}$ and Y denotes the admittance matrix. At this point we need to specify that all rational models we have obtained so far by using Laguerre-Gram were already passive and therefore no correction was needed but the above mentioned solution could easily be used if necessary.

Equivalent circuit model

VLSI circuit designers often use SPICE-based simulation software. It is therefore important to be able to translate a reduced order model into a simple equivalent circuit. Theoretically, it has been proven that if the model is passive it can be implemented by an RLCG physically realizable circuit [8]. Practically however, finding such a circuit is often difficult since we have no a priori information on its design.

But since our purpose is to simulate and not to physically build we have chosen the solution proposed by Liu&al.[3]. We basically state on the structure of the equivalent circuit and then calculate each of its elements. This may lead to negative RLCG values but since the rational model is passive and the procedure is error free the circuit will also be globally passive. For a 2x2 admittance matrix (one line) the general design of the circuit is presented in Fig. 1a, each element y_i of the π quadripole is realised according to Foster's canonical form. For a 4x4 admittance matrix (two coupled lines) [5] we have the general design in figure 1b and it is quite obvious how it should evolve for larger matrices.

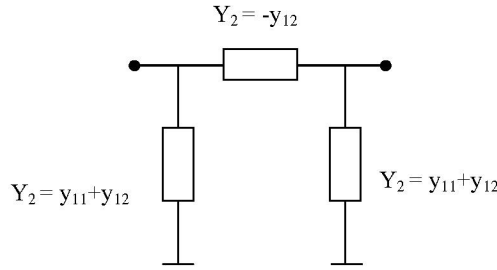


Fig.1a – Equivalent circuit design for one line

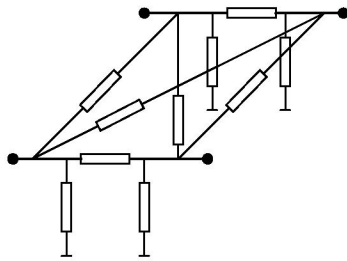


Fig.1b - Equivalent circuit design for two coupled lines

Example

We have chosen the example of a 1.5 mm interconnect line characterized by the following line parameters: $R=72852 \Omega$, $C=100 \text{ pF}$, $L=1.08 \mu\text{H}$ obtained by electromagnetic simulation. In this case the elements of the admittance matrix will be given by

$$Y_{11} = Y_{22} = \frac{ch(\sqrt{ZY})}{Z(\sqrt{ZY})^{-1}sh(\sqrt{ZY})}$$

$$\text{et } Y_{12} = Y_{21} = -\frac{1}{Z(\sqrt{ZY})^{-1}sh(\sqrt{ZY})}$$

where $Z = R + jL\omega$ and $Y = G + jC\omega$ represent the series and respectively parallel contributions of line parameters. We compute an order 12 model according to the iterative algorithm described in [2] and [5]. Its frequency response is compared to the original in figures 2a – 2d. As a general rule the rational approximation matches the irrational original until a certain frequency proportional to its order (tens of GHz in this particular case), weight functions can however be used to favor specific frequencies. This paper essentially focuses on

transient response analysis, a frequency approach on Laguerre-Gram is available in [6].

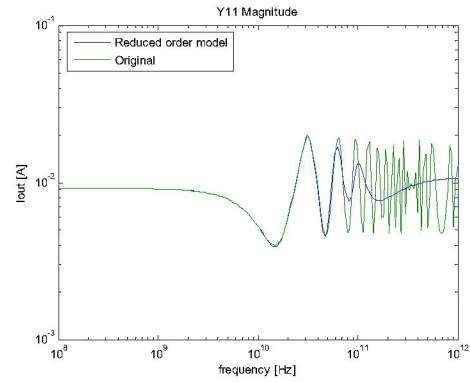


Fig.2a – Y_{11} , magnitude

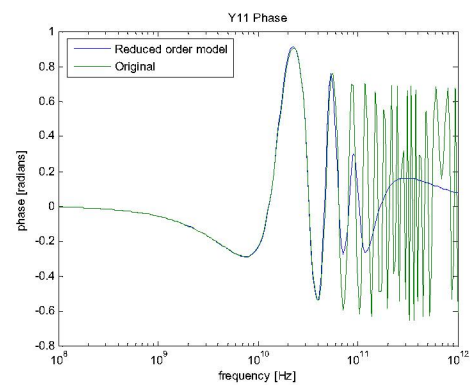


Fig.2b – Y_{11} , phase

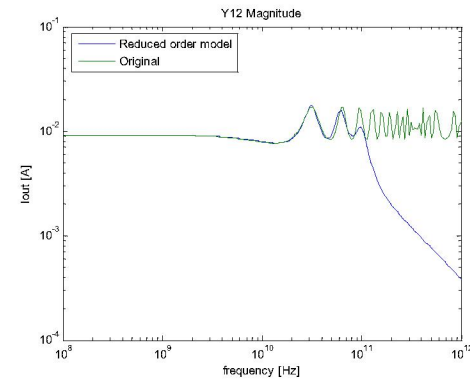


Fig.2c – Y_{12} , magnitude

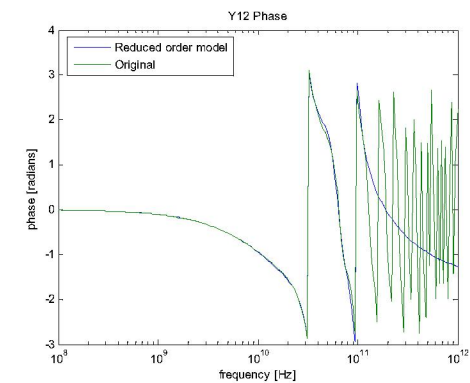


Fig.2d – Y_{12} , phase

The next step is to test passivity. Since the model is passive, it requires no correction and an equivalent circuit may be determined. The design in figure 3 illustrates the cited method (see paragraph IV) and counts a total of 74 RLC components. We have also tested other techniques to design the individual y_i elements (e.g. a generalization of Cauer's method based on continuous fractions) but they lead to an identical complexity.

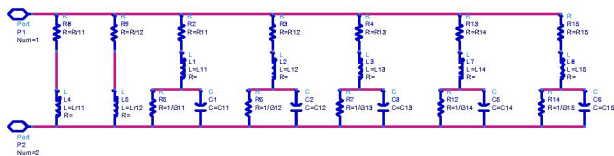


Fig.3a – Equivalent circuit for y_2

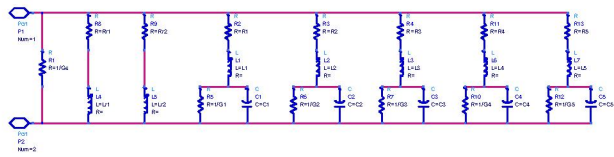


Fig.3b – Equivalent circuit for y_1

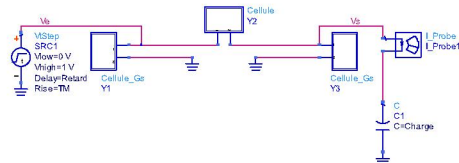


Fig.3c – Complete equivalent circuit with a $5fF$ load

We have then simulated the equivalent circuit under Advanced Design Simulation 2004A with a capacitive load of $5fF$ and compared it to a classical RLC PEEC counting 25 cells (75 elements). The reference model chosen in this example is also a PEEC but with a very high number of cells (1000). In Fig. 4 we can see how the three models respond to a non-delayed $1V$ step excitation with a rise time of $24ps$. The important signal characteristics (delay, rise time, and overshoot) are evaluated (Table I) and the errors are computed for the 25 cell PEEC and for our model respectively (Table II). The delay was defined as being 50% of the final value and the rise time was computed between 10% and 90%.

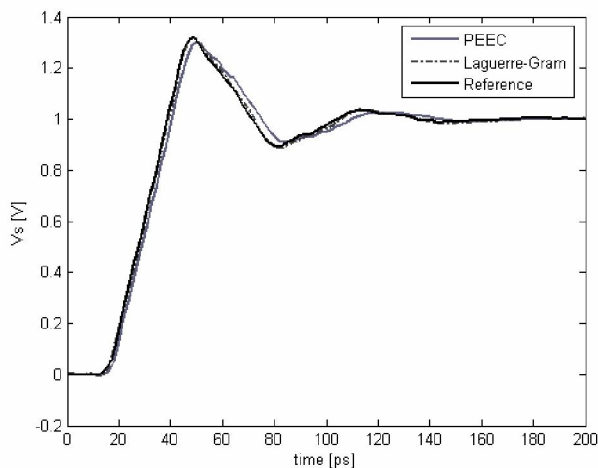


Fig.4 – Transient responses

Model	Delay [ps]	Rise [ps]	$V_{s,max}$ [V]	Overshoot [V]
Reference	27,582	18,159	1,3226	0,3226
Laguerre Gram	27,739	18,495	1,3225	0,3225
PEEC	28,813	18,850	1,2297	0,2297

Table I

Model	Error [%]		
	Delay	Rise	Overshoot
Laguerre Gram	0.57	1,85	0,03
PEEC	4.46	3,80	5.73

Table II

Figure 4 alone is quite relevant to the accuracy of the Laguerre-Gram reduced order model. Its response closely matching the original and Table II confirms the quality of the approximation in terms of delay, rise time, overshoot, parameters essential to circuit designers.

Conclusions

Associating a passivity testing and enforcement technique to the Laguerre-Gram MOR method enables us generate globally passive circuit models which in turn help validate its accuracy on examples such as the one presented in this paper and bring it closer to the practical needs of VLSI circuit designers. We are at this time extending our simulations to more complex examples (several coupled lines) while continuing our search for more efficient rational approximation techniques. We are also interested in comparing our method and other recent work [7].

Acknowledgments

The authors would like to acknowledge Brittany Region's financial support.

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